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Thermal Design of an MCM with the Implanted Temperature Sensor

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Abstract: Since the debut of Multi-chip Modules (MCM), many research and development works have brought the technology from the physical design, test to mass production, but still lacking thermal data to support the schematic designs; especially in the area of thermal design related junction temperature. This method proposes a new approach to implant the temperature sensor into the MCM thus to sense the substrate and to probe the junction temperature. Further, to explore the possibility of using the IEEE1149.7 based cJTAG of the function test in conjunction of the IEEE1149.1 based boundary scan test coherently. This method is to activate a pair of I2C bus as per SCL/SDA lines and to drive and sense the master chip in response of its slave chip. The test platform used in this proposal is to apply the JTAG Technologies based Provision and Core-commander test systems, both of which working together to trouble-shooting and debugging. This is accomplished through manipulating the core logic of the customized IP code amid the Python functions in order to retract the temperature reading from the sensor via the I2C bus. Both JTAG and cJTAG use the common netlist and BSDL files (Boundary Scan Descriptive Language) to generate the test files and firmware coding through the JTAG's Test Access Port (TAP). The formula implemented here has its theoretic roots in a function of the resistance networks which equal to the temperature difference over the the heat flow. This development work uses the high-level GUI language from the core-commander to instruct the Python based functional calls invoking the device drivers, and that has greatly simplified the complex electronic designs with reduced programming, and this exercise has obtained the junction temperature presumably at 71 degrees C on the threshold of temperature gradients, and it's one step closer towards the case temperature from the thermal management point of view.

Keywords: Boundary Scan Test, Multi-chip Module, Thermal Management, Automotive Electronics, JTAG

1. Introduction

Back IBM 370 days, the MCM was a hybrid assembly based on a big ceramic substrate, and that was the backbone of the mainframe. These dies were flipped-over chips so-called dead-bugs on the C4-based bumps. The multiple processors dissipated large amounts of heat and cooled in a helium gas chamber. The mainframes like dinosaurs were dying out once the mini-computers taking over. Subsequently, the servers like mammals raise up to date; however, many die-hard researchers from the IBM's Watson Labs and AT&T's Bell Labs and later at National University of Singapore's Microelectronics Institute (IME), Taiwan's ITRI and Belgium based IMEC Labs, etc., have not given it up and continued on the miniaturization in different ways. Some succeed on the power and RF devices, silicon-on-silicon applications for high-speed digital computing, etc., not until the AMD made a breakthrough to use the chip-lets instead of a big monolithic IC, of which is aided by the TSMC's 7nm wafer fab at lower cost and higher-yielding.

Meanwhile, the nVidia is trying a similar approach on its GPU's integration with plural graphic processors, assembled with the stacked-up DDRs in 3D. Finally, the light at the end of tunnel, when Mr. Elon Musk of Tesla said about the electric vehicles: "a sophisticated computer on wheels", and that has changed the mindset of Intel, Qualcomm and NXP, etc., mainstream chip makers. In parallel progressing, the boundary scan technology has matured, and it has been applied to qualify the MCMs in mass production; however, they are not ready to contest their thermal constrains. These shortcomings have led us to explore the possibility of using the boundary scan test incorporating the function test to probe the critical temperature of the MCM. This is achieved by using only the TCK and TMS other than TDI, TDO, and TRST all five TAP lines to initiate the "active thermal design" towards self-detection. The idea is to implant the MCM with an internal sensor on the substrate, similar to the SoC chip catering the Signature Analysis (SA) for self-diagnostics. By using the JTAG's Core-commander technology, the CPU core manipulates the processor cleverly over-riding the boundary scan registers, this new method uses the Python function to read the sensor outputs via the SCL and SDA lines, resemble a mechanical thermometer picking up the temperature on a thermal couple, their protocols are depicted in the following Table 1 [9, 11, 12].

Table 1. *Junction Temperature Development.*

MCM	Thermal Design using JTAG & cJTAG		
	Provision	**Core-commander**	**Python**
1	Infra Test	Inter Test	Functions
2	Database	GUI	Device drives
3	Schematics	Netlist	Pins
4	Logic	Instructions	Statements
5	Truth Table	Core-logic	Boundary scan
6	Test Vectors	Firmware	Data Container

Some useful considerations in Table 1 are highlighted as follows:

1. Microchip TCN75A I2C (SDL/SCL) related device electronics for temperature sensor 2. Electric schematics of the MCM and its block diagrams based on Altera's FPGA 3. Functional Test based Python coding and firmware programming 4. NXP's i.MAX Dual/6 Quad processors based SoC 5. The tool of JTAG and cJTAG used controller and system software 6. Heat Transfer of an MCM in a nutshell by conduction cooling.

The thermal in this case is managed at the housing which is a clam-shell type design that dissipates the heat to the ambient through its upper cover base of the padding as shown in following Figure 1. [1, 14]

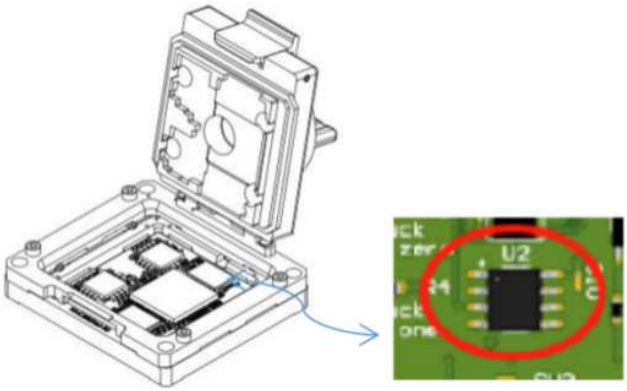


Figure 1. *MCM in a clamshell with an implanted temperature sensor.*

The above design gets popular due to its housing structure installed a lid to secure the MCM during hardware evaluation and firmware programming. In this case, a temperature sensor is represented by the inserted device of U2 in the red circle for prototyping. [3, 13]

2. The MCM Under Case Study

This study introduces a generic MCM depicted in Figure 2, which is typically made of several functional building blocks such as CPU, FPGA, SoC, memories, etc., ICs. The system under evaluation consists of a Cyclone III FPGA from Altera, an ARM-based SoC from NXP and the Microchip's temperature sensor. The following block diagram illustrates an I2C bus, circled in red, which used to prototype this temperature sensor by the JTAG's Provision and Core-commander systems as follows [5, 16].

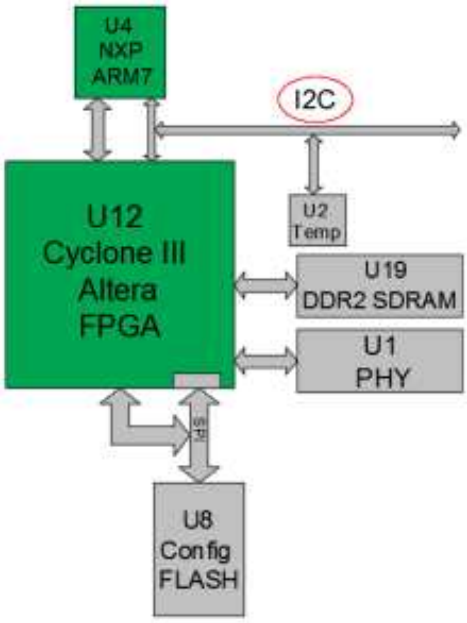


Figure 2. *A temperature sensor of U2 on its I2C bus.*

As shown in Figure 3, a pair of MCMs marked in x and y are assembled on a conduit board to interface the JTAG controller via a digital POD. One for boundary-scan test and one for function test, both depend on a common schematics, netlist and BSDL file. This approach makes this test system versatile to cope with both SoC and FPGA via two daisy-chains of TAP-X and Y in a consolidated database. [2, 15]

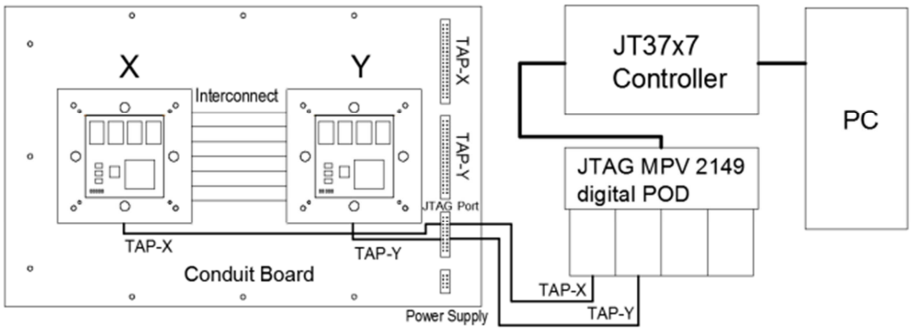


Figure 3. *Test stand for system deployment.*

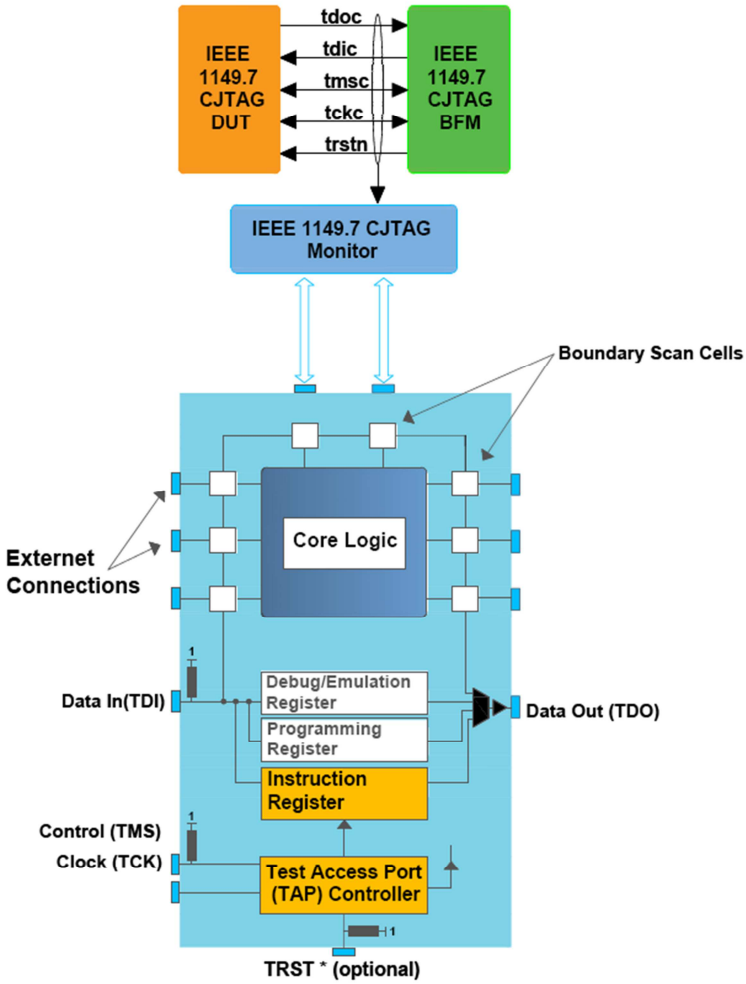


Figure 4. *JTAG & cJTAG working in-sync.*

2.1. Boundary Scan Based Function Test

The above test-stand sets up the JTAG in coherence with the cJTAG test, not only troubleshooting the manufacturing defectives but also debugging the firmware related bugs. It is developed through their shared daisy chain in Figure 3. The daisy chain links the boundary-scan cells serially by TDI and TDO and TCK, TMS in parallel. It can be selected by a switch to run the boundary-scan test or emulation on a click as shown in Figure 3, and simulated in Figure 4 [4].

2.1.1. Temperature Sensor and Thermal Resistance

This study proposes the I2C bus which is an open-source

approach in the application of the master controller to monitor or capture the slave devices as shown in Figure 5, and to take consideration of the temperature difference between the junction and case temperature over the heat flow as expressed in equation (1). Both are applied to evaluate the MCM related thermal performance as follows [10].

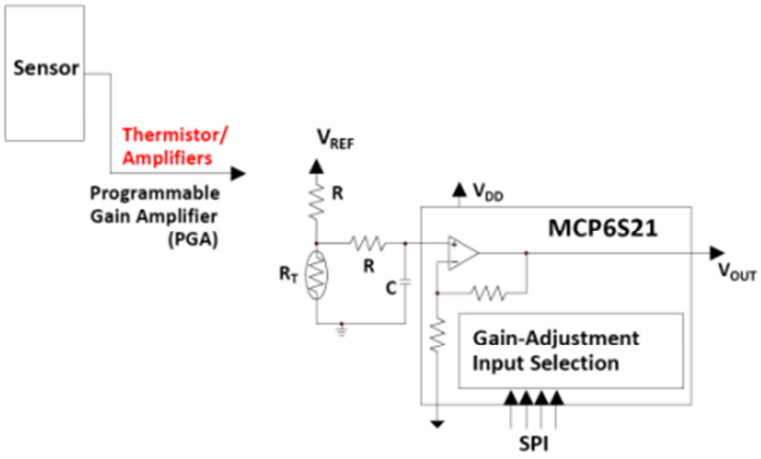
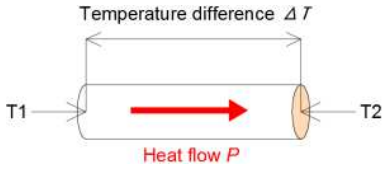


Figure 5. *Sensory electronics at device level.*

Equilibrium condition of the thermal resistance network in relation to the heat flow and the temperature difference between the junction and case, expressed as follows;



$$\text{Thermal resistance } R_{th} = \frac{T1-T2}{Heat\ flow\ P} = \frac{Temperature\ difference\ \Delta T}{Heat\ flow\ P}\ [°C/W] \quad (1)$$

T1: junction, T2: case temperature

2.1.2. Electric Design of the Implanted Temperature Sensor

To implement the above sensor in the circuit design for the master controller as of the SoC with the built-in Arm® Cortex®-M processor, the main IC has pins and nets to interface the I2C based SDA and SCL lines, the circuitry is depicted in Figure 6 below [6].

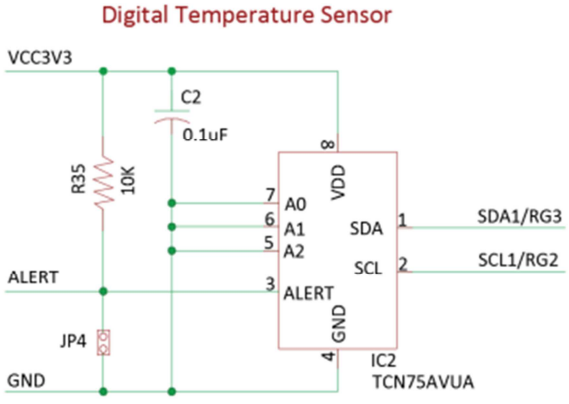


Figure 6. *Electrical design of the sensor.*

2.1.3. Core-commander Related Programming

The Core-Commander applies the high-level GUI to interface the registers and to access the commands in full memory reads and writes. The sequences of the commands can be re-played within the interactive windows or exported to the Python editor. Interactive usage is particularly valuable during hardware booting up and debugging in terms of WriteVar, GetVar, DeclareGroup, WriteGroup, GetGroup, and Get Device Instruction List, etc., instructions. This study applies the programmer's interface so-called "JFTUPROC" with functions for testing and programming in several supported microprocessor cores. [8]

2.2. Firmware Development and Kernels

The Cyclone FPGA embedded development needs the SCIL adapter (Scan Configured Interface Logic) which is the JT 2149/MPV based POD as shown Figure 3. The FPGA is programmed with dedicated firmware (SCIL) to turn them into microcontroller-specific firmware programming, and that can be used in combination with "Ready2Run" software solutions from chip-makers, e.g., Renesas Electronics, NXP, etc. The Core-commander is a programming tool for chips like the SoC, MCU, DSP, etc., activating their emulation mode using the JTAG's TAP pins to invoke the "Kernel-concentric" testing through the Bscan register of IEEE 1149.1 compliant devices. These registers consist of Bscan cells having them integrated into the I/O pins. In these situations, the processor-associated cluster or

peripheral components in programming by means of the Core-Commander is used to manipulate some of the internal ARM-x registers, and to drive the SCL and SDL bus lines under GUI-based macros, as shown in the following scripts in Figure 7.

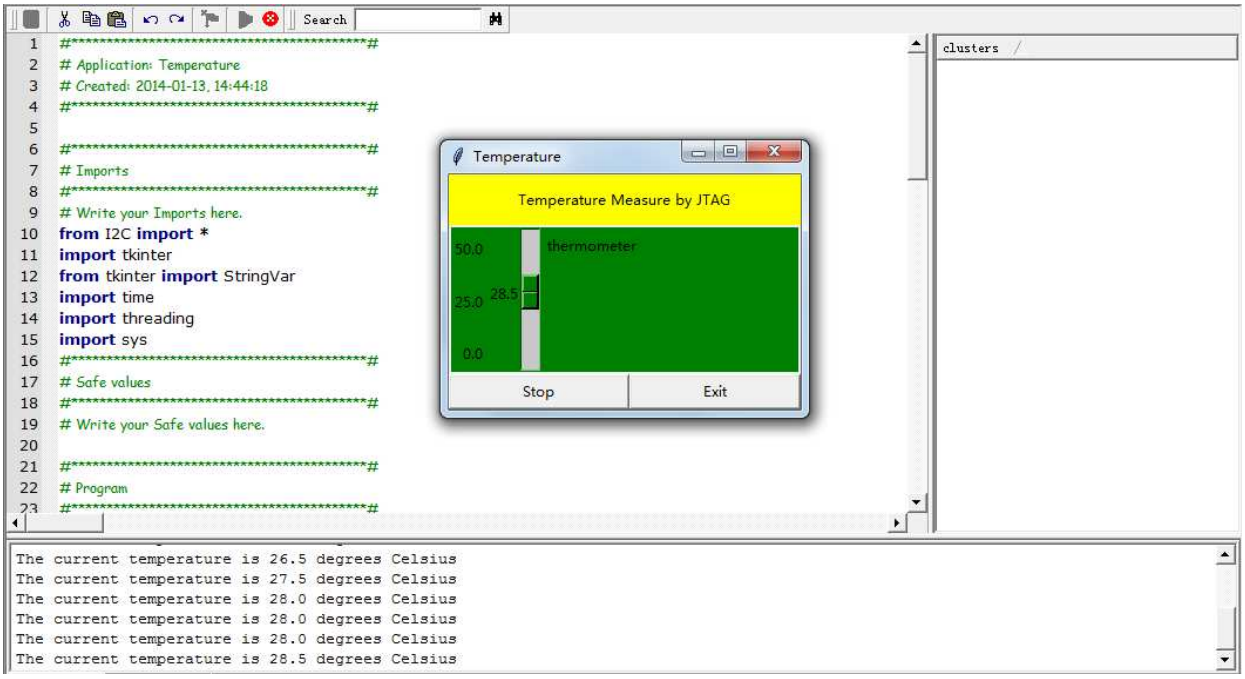


Figure 7. *High level GUI for test code generation.*

3. Junction Temperature Development

The Python function-based firmware programming is first to initiate the keywords, identifiers, statements and commends of which require Python variables and data types. They establish type conversion to define its I/O's and import to their operators. Using these logic commands, the programmer is enabled to run flow control, related operations such as "if-else", "looping", "while", "break", "continue and pass", etc., logic. Subsequently, the function calls for "argument", "recursion", "local and "global nets", "modules", "package", etc., coding are invoked for device drivers. [7]

3.1. Boundary Scan Based Function Test

The Core-commander activates the core-logic to relate the test data with the embedded programming. This test strategy provides a coherent functionalities for the JTAG and the cJTAG to acknowledge the SDA and SCL bus by the Python functions as shown in the following Figure 8.

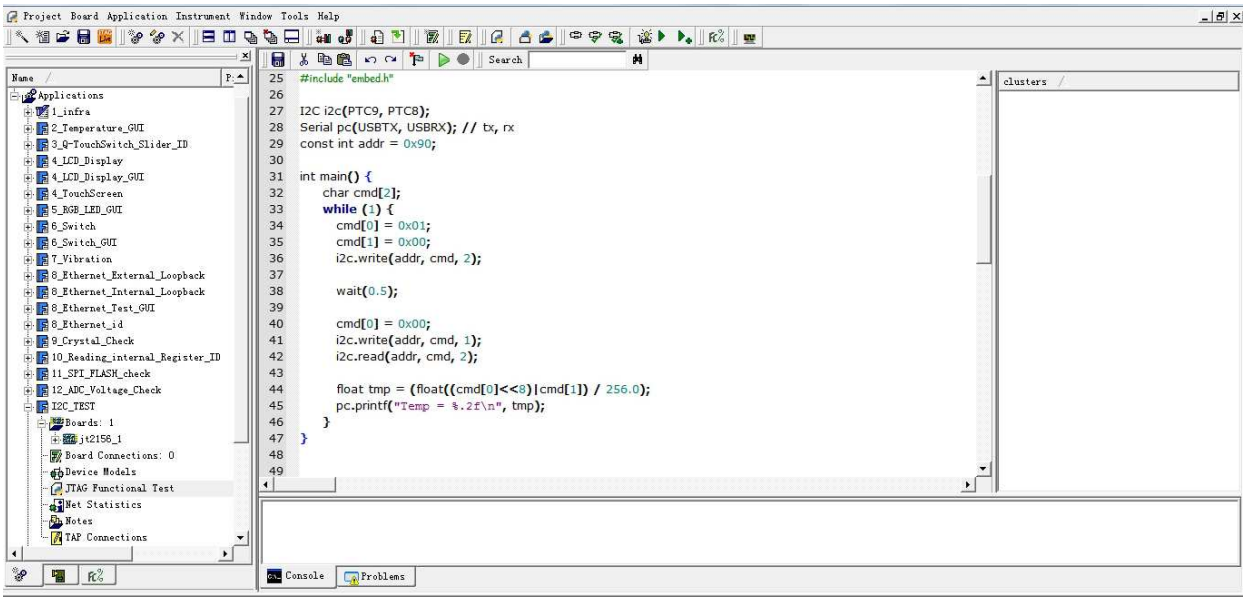


Figure 8. *Firmware Coding for Python Functions.*

3.2. Temperature Gradients Due to Heat Exchange

For the given direction in Eq. 1, the temperature gradient is the rate of change of temperature with respect to the displacement from the hot spot to the heat sink where is the substrate. The term temperature gradient in this case gives the direction from the flip chips to the bumping at a rate of heat dissipation. In other words, for higher thermal conductivity, the temperature gradient is smaller and for lower thermal conductivity, the temperature gradient is higher in terms of the ambient temperature since the MCM is a microelectronic device with very limited thermal conductivity path. [17]

Many years research, the academic has suggested the heat heat sink in an MCM being the ceramic or silicon on silicon for higher thermal conductivity; however, the argument ceased at the polyimide based substrate with dielectric conductivity at k = 2.4 approximately; besides the under-filling of the flip-chips has filled up the thermal gap which is less than 5mm, insignificantly.

Traditional monolith package IC's which enclosed in a plastic package, they are heat isolated on the dies with poor heat dissipation to the case, and which is the reason why the birth of the MCM originally thought, aside from the speed issues. Even though the 2D and 3D packaging in advanced MCMs on drawing board, yet the stack-up dies in the MCM have accumulated highly condensed heat making this type thermal design requires internal thermal sensing capability even more so.

To retract data on the temperature sensor as shown in Figure 9, this function test is to output the temperature profile on the threshold of the temperature gradients before reaching its critical temperature. To keep the junction temperature sustainable at 71 degrees C, this test procedure reports the result of the performance of the temperature sensor on the raising or falling of the device under test as follows:

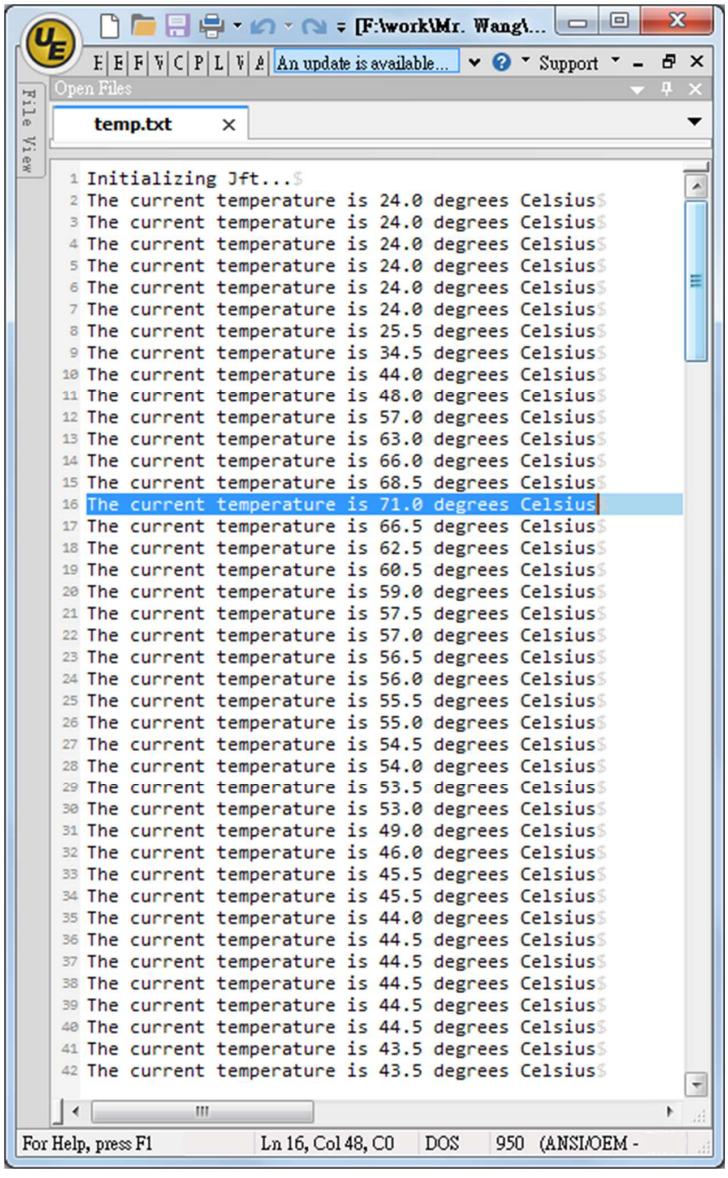


Figure 9. *The junction temperature on the threshold of temperature gradients.*

4. Infra/Interconnection Test

As stated, the original JTAG based boundary scan test could not initiate the core logic on behave of the the boundary scan registers. The Core-commander activates the CPU related core-logic, and the test data using the embedded programming to exercise the emulation and debugging mode. This test strategy provides a coherent approach for the cJTAG coupling with the JTAG through the SDA and SCL lines as shown in Figures 10 and 11, cleverly initiate the function test through Infrastructure and Interconnection test.

4.1. Boundary Scan Based Infrastructure Test

This test is developed to follow the IEEE1149.1 required test protocol and to address the SoC and FPGA related test registers in association with their perspective boundary scan cells as follows.

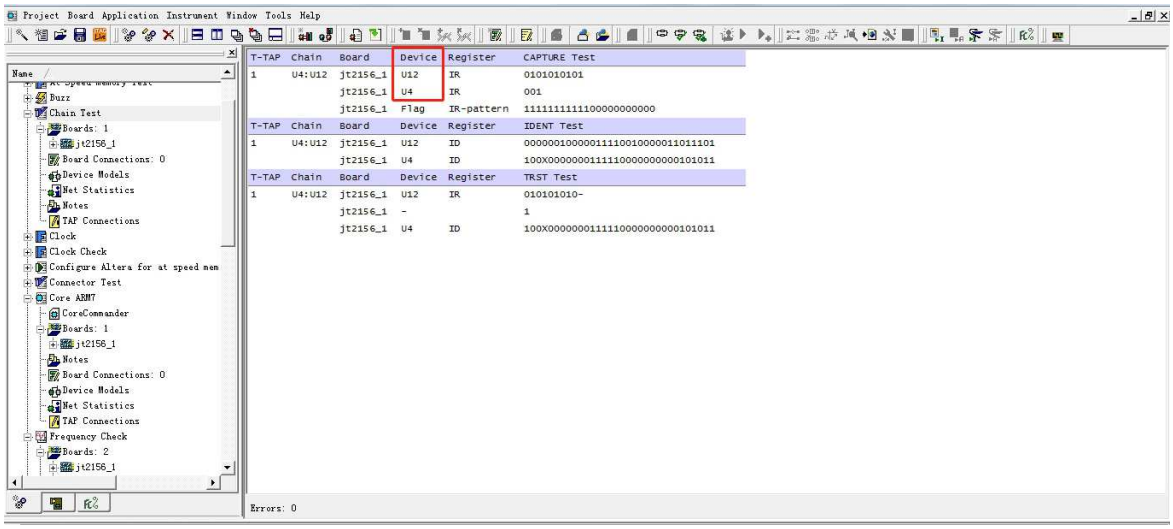


Figure 10. *Infrastructure test set up the SoC and FPGA.*

Specifically, they are capture, bypass of these data and instruction registers, along with the ID in 32-bits registration of the dies. Since this MCM has a connected daisy chain, of which can be separated to classify each chain may have different role in function or boundary scan test, as shown in Figure 10.

4.2. Boundary Scan Based Interconnection Test

Based on the schematics generated netlists, the interconnection test executes cells level analysis through drive and sense the cells on data, address and control bus with respect to their counterpart cells on the chain, of which may be uni-directional, bi-directional or high impedance, interactively diagnose if any cell misbehaves on their data string according to the test instruction, i.e., driving high but sensing "0" or driving "low" but sensing "1". These interconnection related defectives take place at the bumps if shorting or nets if opening in the substrate or grounding, bridging, etc. flaws to be diagnosed on a truth table based vector analysis as shown in Figure 11.

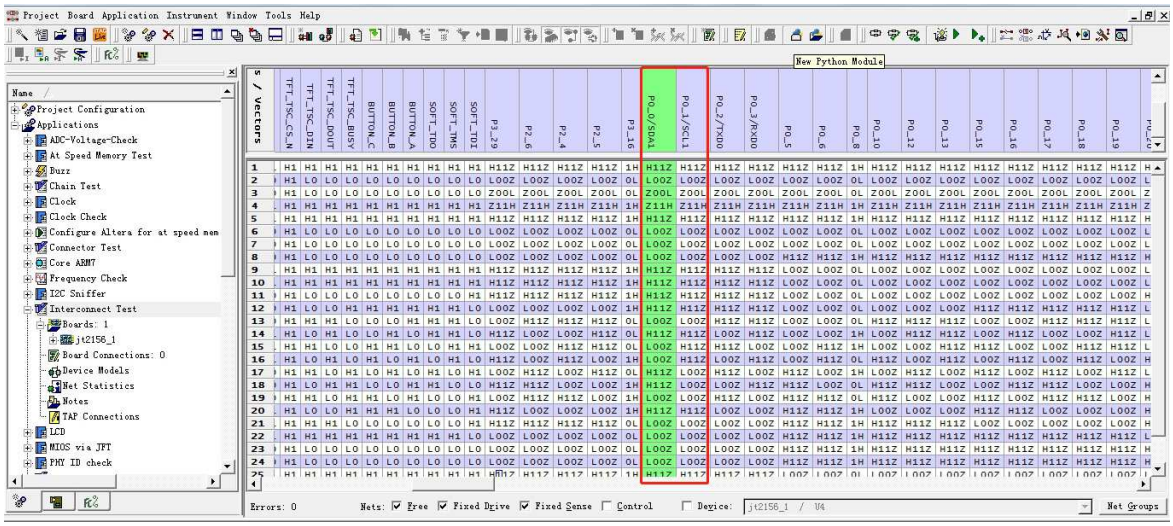


Figure 11. *Interconnection test to pick up the SDA and SCL lines.*

This unique test approach has further incorporated with the function test required sensory lines with the I2C bus among these data, address and control interconnections. There are two implanted control lines as per SCL/SDL remarked in RED as shown in Figure 11, they used to call for the Python functions. As shown in red block, they are embedded in the JTAG (TDI, TDO, TCK, TMS, TRST) based test vectors to read out the temperature sensor on the same truth table with their own boundary scan cells, not only to perform the function test but also make sure their existence in the MCM working on data transmission and receiving sensory signals by cJTAG (TCK/TMS).

5. Conclusion

The main objective of this research is to discover the MCM related junction temperature on the threshold of the temperature gradients. The method proposes an integrated solution for the JTAG and cJTAG based BST and FCT under supervision of the Core-commander and Provision systems. This approach has greatly simplified the complicate electric design and electronics related firmware development in a coherent system. In summary, this study explores the junction temperature as one of the important parameters to contribute the thermal resistance network as a prelude towards the case temperature related total thermal management.

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